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64331 7590 04/20/2007 OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			EXAMINER SUGENT, JAMES F	
			ART UNIT 2116	PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE			MAIL DATE	DELIVERY MODE
3 MONTHS			04/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/750,256

Applicant(s)

O'CONNOR ET AL.

Examiner

James F. Sugent

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 December 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-42 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-42 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received December 21, 2006 and In-Person Interview conducted March 1, 2007 for application number 10/750,256 originally filed December 29, 2003.

Claim Rejections - 35 USC § 101

As was discussed in the Interview conducted March 1, 2007, the Examiner has considered Applicant's arguments in re dependent claims 36 and 37 and rejection presented under 35 USC § 101. The Examiner found the Applicant's arguments persuasive. Therefore, the rejection under 35 USC § 101 has been withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-30 and 34-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Bose et al. (U.S. Patent Publication No. 2004/0221185 A1) (hereinafter referred to as Bose).

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As to claim 1, Bose discloses a method comprising: initiating a power increase for a potentially needed functional unit to an operable power level (Bose discloses a signal [134] sent from a unit-level activity prediction logic [130] to target execution units [118, 120, 122, et al.] to change from a “sleep” or “power-down” state to a “wake up” state; paragraph 37, lines 20-28 and paragraph 38), if the potentially needed functional unit has a present power level that is lower than the operable power level, wherein the potentially needed functional unit is identified based on a determination of whether the potentially needed functional unit is operable to execute at least one software instruction stored within an instruction cache (Examiner would like to take this opportunity to re-define the possible previous understanding of instruction cache in the previous Office Action. Bose discloses “an instruction cache (ICACHE) 102, an instruction fetch address register (IFAR) 104, an instruction buffer (IBUF) 106, multiplexor 108, branch history table and branch target buffer logic BHT/BTB 110, a branch unit 112, an instruction decode-dispatch unit IDU 114 and an issue queue 116 form a typical instruction unit (I-Unit)” wherein said instruction cache is the “instruction unit” and hereinafter referred to as “IUNIT”; paragraph 37) (Bose discloses the prediction logic [130] determining if execution units are needed; paragraph 40, line 1 thru paragraph 41, line 5).

As to claim 2, Bose discloses the method further comprising: fetching one or more software instructions into the instruction cache engine (Bose discloses machine instructions being fetched from an instruction cache 102 but said instructions are inherently fetched from system memory into the instruction cache of a processor and essentially made accessible to a processing engine 130 for prediction/evaluation for power management; paragraph 39, lines 1-24).

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As to claim 3, Bose discloses the method wherein fetching the one or more instructions comprises fetching the one or more instructions into a conventional cache (paragraph 37).

As to claim 4, Bose discloses the method wherein fetching the one or more instructions comprises fetching the one or more instructions into a trace cache (paragraphs 37 and 39).

5 As to claim 5, Bose discloses the method further comprising: fetching a line of one or more software instructions into the instruction cache (Bose discloses machine instructions being fetched from an instruction cache but said instructions are inherently fetched from system memory into the instruction cache of a processor and essentially made accessible to processing engine 130 for prediction/evaluation for power management; paragraph 39, lines 1-24);
10 generating an information vector (132) for the line before or as the line is fetched into the instruction cache, wherein the information vector identifies a set of functional units that are operable to execute the one or more software instructions (paragraph 42); and identifying the potentially needed functional unit based on the information vector (with request signals 134; paragraph 40).

15 As to claim 6, Bose discloses the method further comprising: indicating (signaling) power status information (via signal 134) for a set of functional units (paragraph 40), wherein the power status information indicates whether a functional unit, within the set of functional units, has a present power level that places the functional unit in an operable power state or a low power state (paragraph 40, line 1 thru paragraph 41, line 5).

20 As to claim 7, Bose discloses the method further comprising: incrementing a use counter (168) for a functional unit when a software instruction is fetched into the instruction cache, and

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when the functional unit is operable to execute at least part of the software instruction (paragraphs 46 and 51).

As to claim 8, Bose discloses the method further comprising: decrementing the use counter (168) for the functional unit when the software instruction is eliminated from the instruction cache (paragraph 46 and 50).

As to claim 9, Bose discloses the method further comprising: selecting one or more selected lines of software instructions stored within the cache (paragraph 39, lines 1-3); and identifying (predicting) the potentially needed functional unit as a functional unit that is operable to execute at least one software instruction stored within the one or more selected lines (paragraph 39, lines 3-24 and paragraph 40, line 1 thru paragraph 41, line 5).

As to claim 10, Bose discloses the method further comprising: activating (fetching and processing) a line of software instructions stored within the cache (paragraph 39, lines 1-24); and identifying (predicting) the potentially needed functional unit as a functional unit that is operable to execute at least one software instruction stored within the line (paragraph 40, line 1 thru paragraph 41, line 5).

As to claim 11, Bose discloses the method further comprising: identifying (predicting) an unneeded functional unit as a functional unit that is not operable to execute the at least one software instruction (paragraph 40, line 1 thru paragraph 41, line 5); and initiating (signaling via signal 134) a power decrease for the unneeded functional unit, if the unneeded functional unit has a second present power level that is greater than or equal to a second operable power level (paragraphs 39-40 and paragraph 40, line 1 thru paragraph 41, line 5).

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As to claim 12, Bose discloses the method wherein initiating the power decrease comprises: initiating (signaling via signal 134) the power decrease for the unneeded functional unit after execution is complete of any in-flight instructions (branched) that use the unneeded functional unit (paragraph 37, lines 20-28 and paragraph 42).

5 As to claim 13, Bose discloses the method wherein initiating the power increase comprises: initiating (signaling via signal 134) the power increase for a functional unit selected from a group of functional units that includes one or more floating-point units, multipliers, dividers, shifters, digital signal processors, co-processors, application specific integrated circuits, data processing engines, debug logic blocks, encryption units and key-generation units
10 (paragraph 37).

As to claim 14, Bose discloses the method wherein initiating the power increase comprises: determining a selected operable power level from one of multiple operable power levels ("sleep," "power-down" or "wake up"), wherein the selected operable power level is selected based on an expected result latency; and initiating the power increase to the selected
15 operable power level (paragraphs 28 and 42).

As to claim 15, Bose discloses a method comprising: fetching one or more lines of software instructions into an instruction cache (IUNIT), which is accessible to a processing engine (130) (Examiner would like to take this opportunity to re-define the possible previous understanding of instruction cache in the previous Office Action. Bose discloses "an instruction
20 cache (ICACHE) 102, an instruction fetch address register (IFAR) 104, an instruction buffer (IBUF) 106, multiplexor 108, branch history table and branch target buffer logic BHT/BTB 110, a branch unit 112, an instruction decode-dispatch unit IDU 114 and an issue queue 116 form a

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typical instruction unit (I-Unit)” wherein said instruction cache is the “instruction unit” and hereinafter referred to as “IUNIT”; paragraph 37) (Bose discloses machine instructions being fetched from an instruction cache but said instructions are inherently fetched from system memory into the instruction cache of a processor and essentially made accessible to a processing engine 130 for prediction/evaluation for power management; paragraph 39, lines 1-24); identifying (predicting) potentially needed functional units as functional units that are operable to execute at least one software instruction stored within the instruction cache (Bose discloses the prediction logic [130] determining if execution units are needed; paragraph 40, line 1 thru paragraph 41, line 5 and paragraph 42), wherein a functional unit includes a portion of hardware (118, 120, 122, et al.), which is operable to perform a function in response to special instructions received from the processing engine (paragraph 39, lines 17-24); identifying (predicting) unneeded functional units as functional units that are not operable to execute a software instruction stored within the instruction cache (paragraph 41, lines 1-8 and paragraph 42); initiating a power increase (“wake up” signal via signal 134 from the prediction unit 130) for selected ones of the potentially needed functional units that are in a low power state (paragraph 37, lines 20-28); and initiating a power decrease (“sleep” or “power-down” signal via signal 134 from the prediction unit 130) for selected ones of the unneeded functional units that are in an operable power state (paragraph 37, lines 20-28).

As to claim 16, Bose discloses the method further comprising: generating and storing (concatenated from the instruction fetch address register IFAR field) an information vector (132) for selected ones of the one or more lines, wherein the information vector identifies a set of functional units that are operable to execute software instructions within a line; and wherein

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identifying the potentially needed functional unit is performed based on the information vector (paragraph 42).

As to claim 17, Bose discloses the method wherein fetching the one or more instructions comprises fetching the one or more instructions into a conventional cache (paragraph 37).

5 As to claim 18, Bose discloses the method wherein fetching the one or more instructions comprises fetching the one or more instructions into a trace cache (paragraphs 37 and 39).

As to claim 19, Bose discloses the method wherein initiating the power increase comprises: initiating (signaling via signal 134) the power increase for a functional unit selected from a group of functional units that includes one or more floating-point units, multipliers,
10 dividers, shifters, digital signal processors, co-processors, application specific integrated circuits, data processing engines, debug logic blocks, encryption units and key-generation units (paragraph 37).

As to claim 20, Bose discloses the method wherein initiating the power increase comprises: determining a selected operable power level from one of multiple operable power
15 levels ("sleep," "power-down" or "wake up"), wherein the selected operable power level is selected based on an expected result latency; and initiating the power increase to the selected operable power level (paragraphs 28 and 42).

As to claim 21, Bose discloses a computer-readable medium having program instructions stored thereon to perform a method, which when executed within an electronic system, results in:
20 identifying (predicting) a potentially needed functional unit as a functional unit that is operable to execute at least one software instruction stored within an instruction cache (Examiner would like to take this opportunity to re-define the possible previous understanding of instruction cache

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in the previous Office Action. Bose discloses “an instruction cache (ICACHE) 102, an instruction fetch address register (IFAR) 104, an instruction buffer (IBUF) 106, multiplexor 108, branch history table and branch target buffer logic BHT/BTB 110, a branch unit 112, an instruction decode-dispatch unit IDU 114 and an issue queue 116 form a typical instruction unit (I-Unit)” wherein said instruction cache is the “instruction unit” and hereinafter referred to as “IUNIT”; paragraph 37) (Bose discloses the prediction logic [130] determining if execution units are needed; paragraph 40, line 1 thru paragraph 41, line 5 and paragraph 42); and initiating a power increase (“wake up” signal via signal 134 from the prediction unit 130) for the potentially needed functional unit (118, 120, 122, et al.), if the potentially needed functional unit has a present power level that is lower than an operable power level (paragraph 37, lines 20-28 and paragraph 40, line 1 thru paragraph 41, line 5).

As to claim 22, Bose discloses the computer-readable medium wherein executing the program instructions further results in: fetching a line of one or more software instructions into the instruction cache (Bose discloses machine instructions being fetched from an instruction cache 102 but said instructions are inherently fetched from system memory into the instruction cache of a processor and essentially made accessible to a processing engine 130 for prediction/evaluation for power management; paragraph 39, lines 1-24); generating and storing (concatenated from the instruction fetch address register IFAR field) an information vector (132) for the line, wherein the information vector identifies a set of functional units that are operable to execute the one or more software instructions; and wherein identifying the potentially needed functional unit is performed based on the information vector (paragraph 42).

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As to claim 23, Bose discloses the computer-readable medium wherein executing the program instructions further results in: selecting one or more selected lines of software instructions stored within the cache (paragraph 39, lines 1-3); and wherein identifying (predicting) the potentially needed functional unit includes identifying the potentially needed functional unit as a functional unit that is operable to execute at least one software instruction stored within the one or more selected lines (paragraph 39, lines 3-24 and paragraph 40, line 1 thru paragraph 41, line 5).

As to claim 24, Bose discloses the computer-readable medium wherein executing the program instructions further results in: identifying (predicting) an unneeded functional unit as a functional unit that is not operable to execute the at least one software instruction (paragraph 40, line 1 thru paragraph 41, line 5); and initiating (signaling via signal 134) a power decrease for the unneeded functional unit, if the unneeded functional unit has a second present power level that is greater than or equal to a second operable power level (paragraphs 39-40 and paragraph 40, line 1 thru paragraph 41, line 5).

As to claim 25, Bose discloses the computer-readable medium wherein initiating the power increase comprises: initiating (signaling via signal 134) the power increase for a functional unit selected from a group of functional units that includes one or more floating-point units, multipliers, dividers, shifters, digital signal processors, co-processors, application specific integrated circuits, data processing engines, debug logic blocks, encryption units and key-generation units (paragraph 37).

As to claim 26, Bose discloses an apparatus comprising: one or more functional units (execution units 118, 120, 122); an instruction cache (Examiner would like to take this

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opportunity to re-define the possible previous understanding of instruction cache in the previous Office Action. Bose discloses “an instruction cache (ICACHE) 102, an instruction fetch address register (IFAR) 104, an instruction buffer (IBUF) 106, multiplexor 108, branch history table and branch target buffer logic BHT/BTB 110, a branch unit 112, an instruction decode-dispatch unit IDU 114 and an issue queue 116 form a typical instruction unit (I-Unit)” wherein said instruction cache is the “instruction unit” and hereinafter referred to as “IUNIT”; paragraph 37); a processing engine (130), which is operable to access software instructions stored within the instruction cache (IUNIT), and send one or more special instructions to the one or more functional units in order to execute at least some of the software instructions (Bose discloses machine instructions being fetched from the instruction cache of IUNIT but said instructions are inherently fetched from system memory into the instruction cache of a processor and essentially made accessible to a processing engine 130 for prediction/evaluation for power management; paragraph 39, lines 1-24); and one or more power controllers (150 within 130), which are operable to control (send “sleep,” “power-down,” or “wake up” signals via 134) whether or not an operable power level or a low power level is provided to selected ones of the one or more functional units (paragraphs 40 and 42), based on whether or not selected ones of the one or more functional units are operable to execute at least one software instruction stored within the instruction cache (paragraph 37, lines 20-28 and paragraph 40, line 1 thru paragraph 41, line 5).

As to claim 27, Bose discloses the apparatus wherein at least one of the one or more functional units includes an internal functional unit, which is located on a same chip as the processing engine (Bose discloses the processor being a pipelined processor such that the functional units will contain multiple stage units for processing; paragraphs 37 and 62).

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As to claim 28, Bose discloses the apparatus wherein at least one of the one or more functional units includes an external functional unit, which is not located on a same chip as the processing engine (Any other unit used for processing not found within the processing engine 130; paragraph 37).

5 As to claim 29, Bose discloses the apparatus wherein the instruction cache includes a conventional cache (paragraph 37).

As to claim 30, Bose discloses the apparatus wherein the instruction cache includes a trace cache (paragraphs 37 and 39).

10 As to claim 34, Bose discloses the apparatus further comprising: a predecoder (part of IDU 114), which is operable to evaluate selected ones of the software instructions to determine which functional units will be needed to execute an instruction (paragraph 42).

As to claim 35, Bose discloses the apparatus further comprising: a battery interface, operable to provide power to the one or more functional units (paragraph 6).

15 As to claim 36, Bose discloses the apparatus further comprising: a wireless medium interface, operable to enable signals to be sent to and received over a wireless medium (Bose discloses laptops, portable and mobile systems that commonly have wireless medium interfaces; paragraph 6).

20 As to claim 37, Bose discloses the apparatus further comprising: a network interface, operable to enable signals to be sent to and received from a network (Bose discloses laptops, portable and mobile systems that commonly have network interfaces; paragraph 6).

As to claim 38, Bose discloses the apparatus wherein the one or more functional units comprise: one or more functional units selected from a group of functional units that includes

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one or more floating-point units, multipliers, dividers, shifters, digital signal processors, co-processors, application specific integrated circuits, data processing engines, debug logic blocks, encryption units and key-generation units (paragraph 37).

5

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

10

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

15

Claims 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bose (as cited above) as applied to claim 26 above, and further in view of Theis (U.S. Patent Publication No. 2005/0251621 A1) (hereinafter referred to as Theis).

20

As to claim 31, Bose discloses an instruction cache (IUNIT) with an array (branch history table within 110) but fails to disclose the instruction cache comprising: the array having storage locations; and, a mechanism to sequentially access the storage locations within the array using an enable signal, which has a value that results from shifting information within one or more shift registers.

25

Theis teaches a cache (heap-address cache) that contains an array (stack) of storage locations (addresses) that sequentially accesses (circular stack which sequentially accesses said addresses) using an enable signal (stack pointer or symbolic variable; paragraph 81) that accesses the stack which has a value (count) that results from shifting within one or more shift registers

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(paragraph 218). Theis also has the added benefit of accessing addresses using both conventional machine code as high level programming languages (paragraphs 78-81).

It would have been obvious to one of ordinary skill of the art having the teachings of Bose and Theis at the time the invention was made, to modify the instruction cache (IUNIT) of Bose to include the ability to store and access an array (stack) of addresses sequentially by use of shift registers as taught by Theis. One of ordinary skill in the art would be motivated to make this combination of having an instruction cache that can store and access an array (stack) of addresses sequentially by use of shift registers in view of the teachings of Theis, as doing so would give the added benefit of accessing addresses using both conventional machine code as high level programming languages (as taught by Theis above).

As to claim 32, Theis teaches the apparatus wherein the mechanism to sequentially access the storage locations includes a plurality of first latches, within which a first portion of the enable signal is stored, and wherein the first portion of the enable signal is used to activate a selected word line within the array (Theis teaches the stack of addresses being sequentially accessed by use of a stack pointer which uses a latch [multiplexor] to select the stack item; paragraph 218).

As to claim 33, Theis teaches the apparatus wherein the mechanism to sequentially access the storage locations includes a plurality of second latches, within which a second portion of the enable signal is stored, wherein the second portion of the enable signal is used to select a portion of the selected word line (Theis teaches the stack of addresses being sequentially accessed by use of a stack pointer which uses a latch [multiplexor] to select the stack item; paragraph 218).

Claims 39-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bose (as cited above) in view of Theis (also cited above).

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As to claim 39, Bose discloses an apparatus comprising: one or more functional units (execution units 118, 120, 122); an instruction cache (Examiner would like to take this opportunity to re-define the possible previous understanding of instruction cache in the previous Office Action. Bose discloses “an instruction cache (ICACHE) 102, an instruction fetch address register (IFAR) 104, an instruction buffer (IBUF) 106, multiplexor 108, branch history table and
5 branch target buffer logic BHT/BTB 110, a branch unit 112, an instruction decode-dispatch unit IDU 114 and an issue queue 116 form a typical instruction unit (I-Unit)” wherein said instruction cache is the “instruction unit” and hereinafter referred to as “IUNIT”; paragraph 37); a processing engine (130), which is operable to access software instructions stored within the
10 instruction cache (IUNIT), identify at least one functional unit from the one or more functional units based on a determination of whether the one or more functional units is operable to execute at least one software instruction stored within an instruction cache (with request signals 134; paragraph 40), and send one or more special instructions to the at least one or more functional unit in order to execute at least one of the software instructions (Bose discloses machine
15 instructions being fetched from the instruction cache of IUNIT but said instructions are inherently fetched from system memory into the instruction cache of a processor and essentially made accessible to a processing engine 130 for prediction/evaluation for power management; paragraph 39, lines 1-24).

Bose discloses an instruction cache (IUNIT) with an array (branch history table within
20 110) but fails to disclose the instruction cache comprising: the array having storage locations; and, a mechanism to sequentially access the storage locations within the array using an enable signal, which has a value that results from shifting information within one or more shift registers.

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This teaches a cache (heap-address cache) that contains an array (stack) of storage locations (addresses) that sequentially accesses (circular stack which sequentially accesses said addresses) using an enable signal (stack pointer or symbolic variable; paragraph 81) that accesses the stack which has a value (count) that results from shifting within one or more shift registers (paragraph 218). This also has the added benefit of accessing addresses using both conventional machine code as high level programming languages (paragraphs 78-81).

It would have been obvious to one of ordinary skill of the art having the teachings of Bose and This at the time the invention was made, to modify the instruction cache (IUNIT) of Bose to include the ability to store and access an array (stack) of addresses sequentially by use of shift registers as taught by This. One of ordinary skill in the art would be motivated to make this combination of having an instruction cache that can store and access an array (stack) of addresses sequentially by use of shift registers in view of the teachings of This, as doing so would give the added benefit of accessing addresses using both conventional machine code as high level programming languages (as taught by This above).

As to claim 40, This teaches the apparatus wherein the mechanism to sequentially access the storage locations includes a plurality of first latches (registers), within which a first portion (entry x) of the enable signal is stored, and wherein the first portion of the enable signal is used to activate a selected word line within the array (This teaches the stack of addresses being sequentially accessed by use of a stack pointer which uses a latch [register] to select the stack item; paragraph 218).

As to claim 41, This teaches the apparatus wherein the mechanism to sequentially access the storage locations includes a plurality of second latches (registers), within which a second

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portion (entry y) of the enable signal is stored, wherein the second portion of the enable signal is used to select a portion of the selected word line (Theis teaches the stack of addresses being sequentially accessed by use of a stack pointer which uses a latch [register] to select the stack item; paragraph 218).

5 As to claim 42, Bose discloses the apparatus further comprising: one or more power controllers (150 within 130), which are operable to control (send "sleep," "power-down," or "wake up" signals via 134) whether or not an operable power level or a low power level is provided to selected ones of the one or more functional units (paragraphs 40 and 42), based on whether or not selected ones of the one or more functional units are operable to execute at least
10 one software instruction stored within the instruction cache (paragraph 37, lines 20-28 and paragraph 40, line 1 thru paragraph 41, line 5).

Response to Arguments

Applicant's arguments filed December 21, 2006 have been fully considered but they are
15 not persuasive.

Independent claim 39 was amended to now contain similar limitations that are recited in independent claims 1, 15 and 21. Therefore, claim 39 is rejected under the same arguments presented for claims 1, 15 and 21 as recited in previous Office Action submitted October 25, 2006.

20 As to independent claims 1, 15, 21, and 26, they remain rejected for the same reasons presented in both the last Office Action, submitted October 25, 2006, and reasons covered in the In-Person Interview conducted on March 1, 2007. Therefore, dependent claims 2-14, 16-20, 22-

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25, 27-38 and 40-42 also remain rejected for reasons also in the last Office Action and their dependence on the above independent claims.

Conclusion

5 Any inquiry concerning this communication or earlier communications from the Examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The Examiner can normally be reached on 8AM - 4PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the
10 organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR
15 system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call (800) 786-9199 (IN USA OR CANADA) or (571) 272-1000.

20 James F. Sugent
Patent Examiner, Art Unit 2116
April 6, 2007


REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
4/9/07